MAHESH SHIROLE

Associate Professor, VJTI, Mumbai

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BIOGRAPHY

Mahesh Shirole's teaching and research activities span over 20 years in the areas of software engineering, blockchain technology, networking, etc. Currently, he is Head and Associate Professor of Computer Engineering at Veermata Jijabai Technological Institute (VJTI), Matunga, Mumbai-400 019. He holds a doctoral degree in Computer Engineering from Indian Institute of Technology, Kharagpur (IITKGP), a masters degree in Computer Engineering from VJTI, Mumbai, and a bachelors degree in Computer science and engineering from Walchand College of Engineering, Sangali. Mahesh is a powerful force in the workplace and uses his positive attitude and tireless energy to encourage others to work hard and succeed.

TEACHING

Mahesh has designed and taught numerous courses in Computer Science and Engineering. He has taught core and advanced courses (Data Structures, Algorithms, Database Management Systems, Automaton Theory, Software Engineering, Machine Learning), application courses (Image Processing, Software Architecture), and specialized courses (Blockchain Technology etc.). His teaching style focuses on enhanced student engagement and active learning. He has a strong ability to deliver course material through a variety of teaching methods. Also possess a multitasking ability to balance teaching and administrative duties.

RESEARCH

Mahesh's research interests include software engineering, blockchain technology, machine learning, networking, security, and evolutionary optimization. He has published over 25 research articles in international journal and conferences. He has supervised over 20 master students and currently supervising 3 doctoral students. Four research articles have more than 50 citations. His h-index is 8.

SERVICES

Mahesh has been active member of academic bodies of the institution. He served, for reforms/revisions in curriculum, academic structure, regulations and ordinances. He served as a member of academic committees in Sardar Patel Institute of Technology (SPIT), Bharatiya Vidya Bhavan, Andheri, Mumbai, Shah & Anchor Kutchhi Engineering College, Chembur, Mumbai, etc. He has delivered invited lectures and tutorials in several faculty development programs. He has singlehandedly designed, developed, and implemented First Year Admission Process and enhanced from manual to the automated allotment system during 2003-2005. He has also developed programs for the student registration, 5^{th} pay arrears calculations during 2005-2006. He was a member of academic delegation to Australian Universities in 2008 to understand teaching learning process and possibilities of academic and research collaboration.

STRENGTHS

Hard-working | Persuasive | Motivator

LANGUAGES

Marathi
Hindi
English

ADMINISTRATION

Head CE&IT Department
VJTI, Mumbai
2021-

Controller of Examination
VJTI, Mumbai
2015-17

Faculty In-charge IT Infrastructure
VJTI, Mumbai
2014-15

First Year Admission
VJTI, Mumbai
2001-2005

EDUCATION

PhD in Computer Sci. & Engg.
IIT, Kharagpur, India
2021

M.E. in Computer Engineering
VJTI, Mumbai, India
2004

B.E. in Computer Sci. & Engg.
WCE, Sangali, India
1996

RESEARCH INTERESTS

- Machine Learning
- Blockchain Technology
- Software Engineering
- Networking
- Cyber Security

PUBLICATIONS

Journal Articles

- Shirole, M., & Kumar, R. (2023). Concurrent behavioral coverage criteria for sequence diagrams. *Innovations in Systems and Software Engineering*, *19*(2), 157–176.
- Shirole, M., & Kumar, R. (2021a). Concurrency coverage criteria for activity diagrams. *IET Software*, *15*(1), 43–54.
- Shirole, M., & Kumar, R. (2021b). Constrained permutation-based test scenario generation from concurrent activity diagrams. *Innovations in Systems and Software Engineering*, 1–11.
- Shirole, M., Darisi, M., & Bhirud, S. (2020). Cryptocurrency token: An overview. *IC-BCT 2019*, 133–140.
- Shirole, M., & Kumar, R. (2013). Uml behavioral model based test case generation: A survey. *SIGSOFT Softw. Eng. Notes*, *38*(4), 1–13. doi:10.1145/2492248.2492274
- Shirole, M., & Kumar, R. (2012). Testing for concurrency in uml diagrams. *SIGSOFT Softw. Eng. Notes*, *37*(5), 1–8.

Conference Proceedings

- Khedkar, S., Mahajan, K., & Shirole, M. (2023). Optimization of blockchain based e-voting. In *2023 8th international conference on business and industrial research (icbir)* (pp. 700–705).
- Shah, D., Shah, J., Parmar, A., & Shirole, M. (2022). Ghar seva - a recommendation system with spatial analysis. In *2022 4th international conference on advances in computing, communication control and networking (icac3n)* (pp. 2191–2197).
- Thorve, A., Shirole, M., Jain, P., Santhumayor, C., & Sarode, S. (2022). Decentralized identity management using blockchain. In *2022 4th international conference on advances in computing, communication control and networking (icac3n)* (pp. 1985–1991).
- Dcunha, S., Patel, S., Sawant, S., Kulkarni, V., & Shirole, M. (2021). Blockchain interoperability using hash time locks. In *Proceeding of fifth international conference on microelectronics, computing and communication systems* (pp. 475–487). Springer.
- Ruparel, H., Hosatti, S., Shirole, M., & Bhirud, S. (2021). Secure voting for democratic elections: A blockchain-based approach. In *International conference on communication, computing and electronics systems* (pp. 615–628). Springer.
- Vispute, A., Patel, S., Patil, Y., Wagh, S., & Shirole, M. (2021). Scaling blockchain by autonomous sidechains. In *Proceeding of fifth international conference on microelectronics, computing and communication systems* (pp. 459–473). Springer.
- Suratkar, S., Shirole, M., & Bhirud, S. (2020). Cryptocurrency wallet: A review. In *2020 4th international conference on computer, communication and signal processing (icccsp)* (pp. 1–7). IEEE.
- Darisi, M., Savla, J., Shirole, M., & Bhirud, S. (2019). Stem: Secure token exchange mechanisms. In *International conference on advances in cyber security* (pp. 206–219). Springer.
- Daftary, K., Kapadia, R., Prajapati, D., & Shirole, M. (2018). Routed: A dynamic bus scheduling system. In *2018 IEEE Symposium Series on Computational Intelligence (SSCI)* (pp. 74–82). IEEE.
- Divekar, A., Parekh, M., Savla, V., Mishra, R., & Shirole, M. (2018). Benchmarking datasets for anomaly-based network intrusion detection: Kdd cup 99 alternatives. In *2018 ieee 3rd international conference on computing, communication and security (icccs)* (pp. 1–8). IEEE.
- Dudhal, A., Mathkar, H., Jain, A., Kadam, O., & Shirole, M. (2018). Hybrid sift feature extraction approach for indian sign language recognition system based on cnn. In *International conference on ismac in computational vision and bio-engineering* (pp. 727–738). Springer.
- Narkhede, S., & Shirole, M. (2017). New watermark embedding technique using visual cryptography. In *2017 international conference on energy, communication, data analytics and soft computing (icecds)* (pp. 1786–1790). IEEE.
- Padmanabhan, R., Lobo, K., Ghelani, M., Sujan, D., & Shirole, M. (2016). Comparative analysis of commercial and open source mobile device forensic tools. In *2016 ninth international conference on contemporary computing (ic3)* (pp. 1–6). IEEE.
- Shirole, M., & Kumar, R. (2015). Test scenario selection for concurrency testing from uml models. (pp. 531–536). IEEE.
- Bhaginath, W. R., Shingade, S., & Shirole, M. (2014). Virtualized dynamic url assignment web crawling model. In *2014 international conference on advances in engineering & technology research (icaetr-2014)* (pp. 1–7). IEEE.
- Joshi, G., Shingade, S., & Shirole, M. (2014). Empirical study of virtual disks performance with kvm on das. In *2014 international conference on advances in engineering & technology research (icaetr-2014)* (pp. 1–8). IEEE.
- Shirole, M., Kommuri, M., & Kumar, R. (2012). Transition sequence exploration of uml activity diagram using evolutionary algorithm. In *Proceedings of the 5th india software engineering conference* (pp. 97–100). Kanpur, India: ACM.

- Shirole, M., Suthar, A., & Kumar, R. (2011). Generation of improved test cases from uml state diagram using genetic algorithm. In *Proceedings of the 4th india software engineering conference* (pp. 125–134). Thiruvananthapuram, Kerala, India: ACM.
- Shirole, M., & Kumar, R. (2010). A hybrid genetic algorithm based test case generation using sequence diagrams. In *International conference on contemporary computing* (pp. 53–63). Springer.
- Shah, S., Khandre, A., Shirole, M., & Bhole, G. (2008). Performance evaluation of ad hoc routing protocols using ns2 simulation. In *Conf. of mobile and pervasive computing*.