VEERMATA JIJABAI TECHNOLOGICAL INSTITUTE

H. R. MAHAJANI ROAD, MATUNGA, MUMBAI-400 019

Tender Notice No.: **ELECT/Research & Development/CoE/Embedded/2021**

Tender of Equipment required for CoE Lab of Electrical Engineering Department of the institute.

Separate sealed tenders are invited by the Director, Veermata Jijabai Technological Institute (V.J.T.I.), for supply, installation and commissioning of equipment required for UG laboratories of Electrical Engineering Department. Specifications, terms and conditions of the tender are in the document which can be obtained from VJTI website (www.vjti.ac.in). Each sealed tender should be accompanied by a receipt of online payment of Rs.1,770 /- (Tender Fee plus 18% GST non-refundable) towards the tender processing fee and an earnest money deposit of Rs.7,500/-. The above online payment of **Rs.9,270/-** should be done through SBI CONNECT (http://onlinesbi.com). Tenders received without earnest money deposit will not be considered at all.

Director

Due Date for Tender Submission: 6th August 2021

VEERMATA JIJABAI TECHNOLOGICAL INSTITUTE

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Terms and Conditions of Tender

1. Tenderers are required to study the attached technical specifications and should quote for the suitable items and services by providing two sealed packets I and II as follows;

1.1 Packet (I) should provide full technical specifications of the items. They should further clarify the following points:-

i. Whether item proposed to be supplied satisfies the specification and requirements.

ii. Tenderer should clearly indicate the accessories that are included in the offer for the item.

iii. The additional accessories which can be included separately indicating their need/use. Those additional accessories which are essential for the basic functioning should be marked as Essential and others as Optional.

iv. Tenderer should clearly indicate the period of delivery of the equipment in full.

v. The tenderer quoting should be prepared to substantiate the performance claims if called for, through demonstration at our premises at the Tenderer's cost. All costs related to such demonstration will be borne by the tenderer.

vi. Each packet should be marked on the outside as:

Tender for supply of -

'Equipment required for CoE Lab of Electrical Engineering Department, VJTI PACKET I TENDER NOTICE NO: '**ELECT/Research & Development/CoE/Embedded/2021**'.

1.2 Packet (II) is meant for the financial Bid which should include the following details:-

i. The Tenderer should provide total cost of each item as per the attached specifications giving break-up as

a) Basic cost of item

b) Cost of other accessories

c) Details of taxes and any other cost relevant

ii. Tenderer should indicate separately the cost of any additional accessories Essential and Optional nature

iii. Any claims for additional cost at later stage for the whatever reason will not be tenable

iv. Each such packet (II) should indicate the terms and conditions of payment desired by the tenderer. It should be noted that the institute does not have a policy of giving any advance payment.

v. The cost quoted by the supplier should be valid at least for a period of 90 days after the last date of tender.

vi. This packet (II) should be marked on outside as:

Tender for supply of-

'Equipment required for CoE Lab of Electrical Engineering Department, VJTI PACKET I TENDER NOTICE NO: '**ELECT/Research & Development/CoE/Embedded/2021**'.

vii. Separate cost shall not be paid for installation and commissioning of the equipment.

2. Financial Bids presented in Packet (II) of only those who completely qualify on the basis of "Technical Specification given in Packet (I)" and who have paid the earnest money deposit and tender processing fee will be opened. Financial Bids of those tenderer whose technical bids are not responsive will not be considered.

3. Every tenderer will make an Earnest Money Deposit of Rs. 7,500/- at the time of submitting the tender, by online payment through SBI CONNECT and submit the receipt of payment along with the tender in a separate envelope. The EMD will be refunded after the finalization of the tender except for the vendor whose tender is accepted, where it will be kept as security deposit for a period of three months after the delivery and satisfactory working of the equipment.

4. Steps to be followed for making online payment through "STATE BANK COLLECT"

- Log On to https://www.onlinesbi.com
- Home Page STATE BANK COLLECT
- Click on State Bank Collect
- Click Checkbox to Accept 'Terms & conditions'
- Then click on 'Proceed'
- Select State as 'Maharashtra'
- Select Type of Category as 'Educational Institutions'
- Click on 'Go'
- Select the Name of the institution as 'Veermata Jijabai Technological Institute'.
- Select the 'Payment category' 'EMD and/or Tender Processing Fee' on next screen Enter Name Of firm, Place, PAN, GST No., Enter appropriate Tender Number, Enter appropriate EMD or Tender Fees Amount in Rupees.
- Proceed as instructed and Click on 'Submit'.

- On next screen verify details and click on 'Confirm'.
- You will be taken to payment gateway.
- Select appropriate payment mode.
- Check the charges/commission applicable for selected 'Mode of Payment'.
- Follow instructions to Print Challan and pay at any branch of SBI Bank in Cash / Pay 'online'Using Internet Banking / Credit / Debit card.
- Print e-receipt and submit along with Tender.
- Mandatory RTGS /NEFT form should be attached with online receipt for refund purpose.

5. **Sealed tender should be submitted in office hours at the address mentioned below -**
   Tender should be submitted at the Inward Section, Veermata Jijabai Technological Institute, Main Building 1st floor, H. R. Mahajani Marg, Matunga, Mumbai 400 019.
6. In case the items are not supplied within the specified period, after the placement of the order, the EMD shall be forfeited.
7. The tenderers should furnish all the relevant information in the above mentioned manner.
8. It should be noted that Director, VJTI reserves the right to accept/reject the tender in full without assigning any reasons.
9. The tender, whose tender is accepted, has to provide a comprehensive warranty on all items for five years.
10. Delivery and installation should be at the Electrical Engineering department. V.J.T.I Matunga, Mumbai premises.
11. Placed order is liable to be cancelled if the delivery terms are not honored.
12. The period of validity of the quotation should be at least 90 days.
13. Warranty Period for all equipments should be minimum 5 years or more.
14. The Institute reserves the right to reject any offer without disclosing reason thereof.
15. Quotations received after the due date will not be considered.
16. Additional accessories required for successful performance of the equipment should be clearly indicated with a cost along with the quotations otherwise offer will not be considered.
17. Required three sets of following documentations in English: (along with equipment delivery)
    - Operating and Programming Instruction.
    - Installation and Commissioning instructions.
    - Quality Test Records.
    - Detailed invoice and packing list of all items and devices and detailed prospect of all equipments & all other Accessories to be enclosed in the respective boxes.

Specifications of Boards:

Sr.No.	Item Description	Qunatity
1	**Side Channel & Glitching Starter Pack Level 2**	1
	Includes the following accessories: • ChipWhisperer-Lite Capture • CW308 UFO Baseboard • CW308T-XMEGA Target (XMEGA, AVR Core) • CW308T-STM32F3 Target (Cortex M4) • CW308T-STM32F0 Target (Cortex M0) • CW308T Generic PCB (0.1" spacing prototype board) • CW308T-STM32F Blank PCB • SMA Tee adapter (for power analysis & fault injection simultaneously) • H-Field Probe • Differential Probe • Probe Power Supply (DC-DC) • SMA cables • SMA to BNC cable • 5.0V wall adapter for probe power supply & CW308 Power (if using stand-alone).	
2	**Side Channel & Glitching Starter Pack Level 1**	2
	Includes the following accessories: • ChipWhisperer-Lite Capture • CW308 UFO Baseboard • CW308T-XMEGA Target (XMEGA, AVR Core) • CW308T-STM32F3 Target (Cortex M4) • CW308T-STM32F0 Target (Cortex M0) • CW308T Generic PCB (0.1" spacing prototype board) • CW308T-STM32F Blank PCB • 2x Lifter tool to remove targets • SMA Tee adapter (for power analysis & fault injection simultaneously). • SMA cables • SMA to BNC cable	
3	**ChipWhisperer-Lite (CW1173) Two Part Version**	2
	• ADC Specifications: 10-bit ADC, 105 MS/s maximum sample rate. • ADC Sample Clock Source: Internal generator, external input (direct	

	or with 4x multiplier or phase adjuster). • Analog Input: AC-Coupled, up to +55dB adjustable gain. • GPIO Types: Serial, clock, logic line (i.e., for reset pin). • GPIO Voltage: 3.3V. • Clock Generation Range: 5-200 MHz. • Clock Output Type: Regular, with glitch inserted, only output glitch. • Glitch Width (min) :~4nS (depends on cabling used for routing glitch output). • Glitch Offset: Adjustable in < 200pS increments. • Voltage glitch type: High-power and low-power crowbar circuitry. • Crowbar pulse current: 20A. • USB Interface: Custom open-source USB firmware, up to 25 MB/s speed. • Sample Buffer Size: 24 573. • Target Device: Atmel XMEGA128D4 (on classic device). STM32F303RCT7 on Arm variant. • Programming Protocols: Atmel ISP (for AVR), Atmel PDI (for XMEGA), STM32Fx Bootloader	
4	**ChipWhisperer-Nano-CW1101**	**3**
	• ADC Specifications: 8-bit ADC, 20 MS/s maximum sample rate. • ADC Sample Clock Source: Selectable between internal generator or external input. • Analog Input: AC-Coupled, fixed gain. • GPIO Types: Serial, clock, logic line (i.e., for reset pin). Fixed pin functions. • GPIO Voltage: 3.3V. • Clock Options: 3.75 MHz, 7.5 MHz, 15 MHz, 30 MHz , 60 MHz • Clock Output Type: Generated by microcontroller, clock only (no clock glitching support). • Trigger Type (ADC + Glitch): Rising edge only. • Glitch Width (min): ~20nS (depends on cabling used for routing glitch output). • Glitch Offset: ~200nS jitter, adjustable in 10nS increments. • Voltage glitch type: Low-power crowbar circuitry. • Crowbar pulse current: 4A. • USB Interface: Custom USB firmware (full-speed USB 2.0 device). • Sample Buffer Size: 50 000. • Target Device: STM32F030F4P6 or STM32F070	

	• Programming Protocols: STM32Fx Bootloader	
5	**ESP32 Target Board for CW308**	3
	• SPI Flash chip includes bidirectional buffer to allow: (a) programming of on-board SPI flash chip with external programmer. (b) sniffing SPI traffic without loading data lines (c) triggering on SPI traffic. • Example implementation of SimpleSerial using hardware AES core provided with ESP32 build system. • Can monitor either the VDD_CPU and VDD_RTU supplies using an optional jumper. • ESP32 built in serial bootloader allows programming device using only a USB-Serial cable (included). This allows programming of both external (SPI Flash) and internal (EFUSE) memory.	
6	**Spartan 6 LX9 FPGA Target for CW308**	3
	• Xilinx XC6SLX9-2TQG144C supported. • Perform clock and voltage glitching right from ChipWhisperer-Lite or ChipWhisperer-Pro. • Optional SPI flash footprint allows use of board with non-volatile bitstream support. • Test hardware peripherals, FPGA soft-core processors, and unique hardware encryption designs • JTAG Programmer required for use	