



Veermata Jijabai Technological Institute (V.J.T.I)
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Programme: Diploma in Electronics Engineering (DEInE)

Semester: III

Implemented from: 2017

COURSE CODE	COURSE	G R	TEACHING SCHEME (HRS/WK)				EXAMINATION SCHEME												
			L	T	P	C R	PAPER HRS	TH		IST	TOTAL		PR		OR		TW		TOTAL MARKS
								Max	Min		Max	Min	Max	Min	Max	Min			
173MA31e	Mathematics III	A	3	1		4	3	80	32	20	100	40					25@	10	125
173EX32	Network Analysis	C	3	1	2	6	3	80	32	20	100	40	25**	10			25@	10	150
173EX33	Electronics I	C	3		2	5	3	80	32	20	100	40	50**	20			25@	10	175
173EX34	Measuring Instruments	C	3		2	5	3	80	32	20	100	40			25**	10	25@	10	150
173EX35	Integrated Circuits	C	3		2	5	3	80	32	20	100	40	25**	10			25@	10	150
173EX36	Electronics Workshop	C	1		2	3							25**	10			25@	10	50
173EX37	Development of Life Skill	A			2	2											25@	10	25
173EX38	Development of Professional practice	B			2	2											25@	10	25
TOTAL			16	02	14	32		400		100	500		125		25		200		850

Abbreviations: B - Basic; C - Core; A - Applied; M - Management; L - Theory Lecture; T - Tutorial; P - Practical; TH - Theory Paper; IST - In-Semester Test
 Practical Exam; OR - Oral Exam; TW- Term Work.

PR -

* assessment by Internal Examiner ** assessment by External Examiner @ : TW assessment by Internal Examiner


Curriculum Coordinator


Head
Diploma in Electronics Engg.


Dean - Diploma

